

What is claimed is:

1. A delay locked loop circuit having a duty cycle corrector, the delay locked loop circuit comprising:

5 a phase detector that detects a phase difference between an external clock signal and feedback internal clock signals and generates up-signals and down-signals corresponding to the phase difference;

a first control circuit that, in response to the up-signals and the down-signals, generates first control signals for coarse locking of the phase difference between the external
10 clock signal and the feedback internal clock signals and generates second control signals for fine locking of the phase difference;

a second control circuit that, in response to the up-signals and the down-signals, generates third control signals for coarse duty error correction of the external clock signal and generates fourth control signals for fine duty error correction of the external clock signal; and

15 a delay line unit that includes a plurality of delay cells connected in series, delays the external clock signal through the delay cells, selects output signals of first delay cells from the plurality of delay cells in response to some of the first control signals, selects output signals of second delay cells from the plurality of delay cells in response to others of the first control signals, and selects output signals of third delay cells from the plurality of delay cells
20 in response to the third control signals.

2. The delay locked loop circuit of claim 1, wherein some of the first control signals relate to a rising edge of the external clock signal, and the remaining signals of the
25 first control signals relate to a falling edge of the external clock signal.

3. The delay locked loop circuit of claim 2, wherein some of the second control signals relate to a rising edge of the external clock signal, and the remaining signals of the second control signals relate to a falling edge of the external clock signal.

30 4. The delay locked loop circuit of claim 3, wherein the first control circuit comprises:

a rising edge control circuit that, in response to an up-signal and a down-signal that relate to the rising edge, generates control signals that relate to the rising edge among the first

control signals and generates control signals that relate to the rising edge among the second control signals; and

5 a falling edge control circuit that, in response to an up-signal and a down-signal that relate to the falling edge, generates control signals that relate to the falling edge among the first control signals and generates control signals that relate to the falling edge among the second control signals.

5. The delay locked loop circuit of claim 3, wherein the second control circuit comprises:

10 a first duty correction control circuit that, in response to the up-signals and the down-signals, generates an up-signal and a down-signal for duty correction; and,

a second duty correction control circuit that, in response to the up-signal and the down-signal for duty correction, generates the third control signals and the fourth control signals.

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6. The delay locked loop circuit of claim 5, wherein the up-signal for duty correction is activated when both the up-signal that relates to the rising edge and the up-signal that relates to the falling edge are activated.

20 7. The delay locked loop circuit of claim 5, wherein the down-signal for duty correction is activated when both the down-signal that relates to the rising edge and the down-signal that relates to the falling edge are activated.

25 8. The delay locked loop circuit of claim 1, wherein the third delay cells are selected in the center between the first delay cells and the second delay cells.

9. The delay locked loop circuit of claim 1, further comprising:
a first phase interpolator that, in response to some of the second control signals, interpolates the output signals of the first delay cells, generates a first output signal and a second output signal, provides the first output signal to the phase detector as one of the feedback internal clock signals, and outputs the second output signal as a first internal clock signal;

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a second phase interpolator that, in response to others of the second control signals, interpolates the output signals of the second delay cells, generates an output signal, and

provides the output signal to the phase detector as another one of the feedback internal clock signals; and

a third phase interpolator that, in response to the fourth control signals, interpolates the output signals of the third delay cells, generates an output signal, and outputs the output
5 signal as a second internal clock signal.

10. The delay locked loop circuit of claim 9 further comprising:
a compensation delay that receives the first output signal of the first phase interpolator and the output signal of the second phase interpolator, delays them for a predetermined amount of
10 time, and outputs the delayed first output signal of the first phase interpolator and the delayed output signal of the second phase interpolator to the phase detector.

11. The delay locked loop circuit of claim 9, wherein, after locking, the rising
15 edge of the first output signal of the first phase interpolator is finely synchronized with the rising edge of the external clock signal.

12. The delay locked loop circuit of claim 9, wherein the second output signal of
the first phase interpolator has a pulse that is generated in response to the rising edge of the first output signal of the first phase interpolator after locking.

13. The delay locked loop circuit of claim 9, wherein, after locking, the rising
edge of the output signal of the second phase interpolator is finely synchronized with the falling edge of the external clock signal.

14. The delay locked loop circuit of claim 9, wherein the output signal of the third
phase interpolator has a pulse that is generated in response to the falling edge of the signal whose duty is corrected after locking.

15. A method of correcting a clock signal duty cycle in a delay locked loop circuit
30 having a delay line unit that includes a plurality of delay cells connected in series, the method comprising:

(a) detecting a phase difference between an external clock signal and feedback internal clock signals, and generating up-signals and down-signals corresponding to the phase difference;

(b) in response to the up-signals and the down-signals, generating first control signals for coarse locking of the phase difference between the external clock signal and the feedback internal clock signals and generating second control signals for fine locking of the phase difference each of the first and second control signals comprising some signals that relate to the rising edge of the external clock signal and some signals that relate to the falling edge of the external clock signal;

(c) in response to the up-signals and the down-signals, generating third control signals for coarse duty error correction of the external clock signal and fourth control signals for fine duty error correction of the external clock signal;

(d) selecting output signals of first delay cells from the plurality of delay cells in response to the first control signals that relate to the rising edge, selecting output signals of second delay cells from the plurality of delay cells in response to the first control signals that relate to the falling edge, and selecting output signals of third delay cells from the plurality of delay cells, between the first delay cells and the second delay cells, in response to the third control signals;

(e) interpolating the output signals of the first delay cells in response to the second control signals that relate to the rising edge to generate a first output signal and a second output signal, and providing the first output signal as one of the feedback internal clock signals and outputting the second output signal as a first internal clock signal;

(f) interpolating the output signals of the second delay cells in response to the second control signals that relate to the falling edge to generate an output signal, and providing the output signal as another one of the feedback internal clock signals; and

(g) interpolating the output signals of the third delay cells in response to the fourth control signals to generate an output signal, and outputting the output signal as a second internal clock signal.

16. The method of claim 15, wherein step (c) comprises:

(c1) generating an up-signal and an down-signal for duty correction in response to the up-signals and the down-signals; and

(c2) generating the third control signals and the fourth control signals in response to the up-signal and the down-signal for duty correction.

17. The method of claim 16, wherein the up-signal for duty correction is activated when both the up-signals that relate to the rising edge and the up-signals that relate to the falling edge are activated.

5 18. The method of claim 16, wherein the down-signal for duty correction is activated when both the down-signals that relate to the rising edge and the down-signals that relate to the falling edge are activated.